Abstract of the Disclosure

A semiconductor memory device includes a clock enable signal self refresh buffer for generating a self refresh clock enable signal by receiving the clock enable signal in the self refresh mode, an internal clock signal generating unit for generating an internal clock signal by receiving the external clock signal, a signal synchronization unit for generating an internal clock enable signal by synchronizing the clock enable signal with the internal clock signal, a level detection unit for generating a level detection signal by detecting levels of the internal clock enable signal and the self refresh clock enable signal, a clock self refresh buffer for receiving the external clock signal during a self refresh mode in response to the level detection signal, and a self refresh command generation unit for activating a self refresh command in response to the level detection signal and inactivating the self refresh command in response to the level detection signal and an output signal of the clock self refresh buffer.